SYSTEM CONFIGURATION GENERATE

CONFIGURATION OF TEST HEAD

PIN CONFIGURATION   1. 512DR+ 3201/0(QUARTER)

    2. 1024DR+6401/0 HALF)

    3. 2048DR+12801/0FULL   [1-3] . . . . . >3

CONFIGURATION OF TEST HEAD

PE BOARD   0. NOT EXIST

    1. EXIST

DR PIN	1A1	1A5	17A1	25A1
CHILD A,B . . . . >	1	1	1	1
CHILD C,D . . . . >	1	1	1	1
CHILD E,F . . . . .>	1	1	1	1
CHILD G,H . . . . >	1	1	1	1

IO PIN	33A1	97A1	33A5	97A5
CHILD A,B . . . . >	1	1	1	1
CHILD C,D . . . . >	1	1	1	1
CHILD E,F . . . . .>	1	1	1	1
CHILD G,H . . . . >	1	1	1	1

CONFIGURATION OF DPU

    DC   CONFIGURATION [1-128] . . . . >1-128

    PPS   CONFIGURATION [1-256]] . . . . >1-256

AC FREQUENCY (Hz)   [50,60] . . . .> 60

CONFIGURATION OF FTU

    FLASH OPTION   [Y, N] . . . . [YES]

CONFIGURATION OF FM

    NUMBER OF FMRA BOARD   [0, 8] . . . .> 8
    SIZE OF FMRA BOARD   [1:8G, 2:16G] . . . .>2
    PM (PATTERN MEMORY) BOARD EXIST   [Y, N] . . . .> NO

CONFIGURATION OF MRA

   MRA4 EXIST [Y,N] . . . . > YES

RCPU STN1 A-D EXIST [Y,N] . . . . > YES

RCPU STN1 E-H EXIST [Y,N] . . . .> YES